Instruction Scheduling and Register Allocation on ARM Cortex-M

Ko Stoffelen

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Problem

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But how?

Old problems in CS

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Given program as CPU instructions, reorder them to minimize pipeline stalls (without changing semantics)

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Problems are hard (NP-complete), intensively studied, and related

Classic approach A: Chaitin-Briggs

- Original idea in 1981 [CAC+81, Cha82], many improvements later

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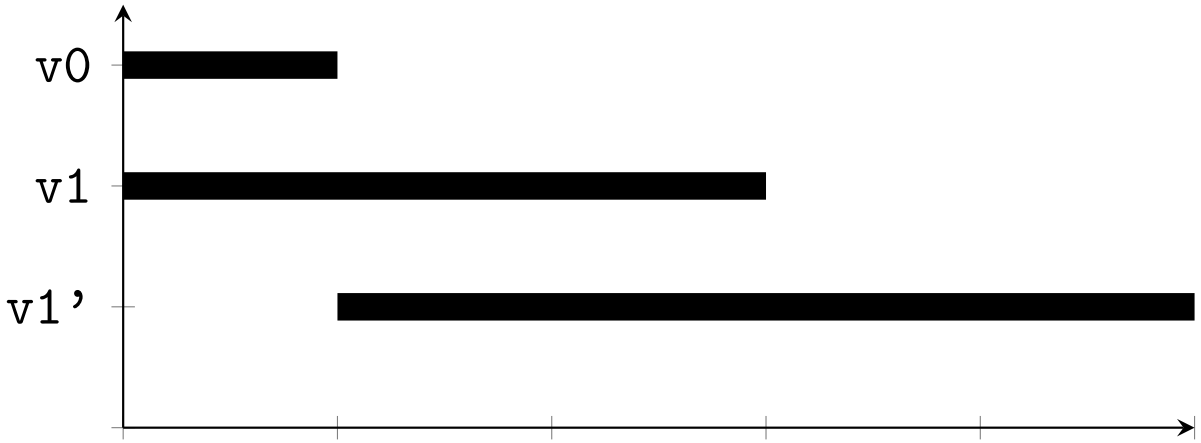
- Write program in *SSA form* to allocate *live ranges*

  `v1 = v1 + v0` $\mapsto$ `v1' = v1 + v0`



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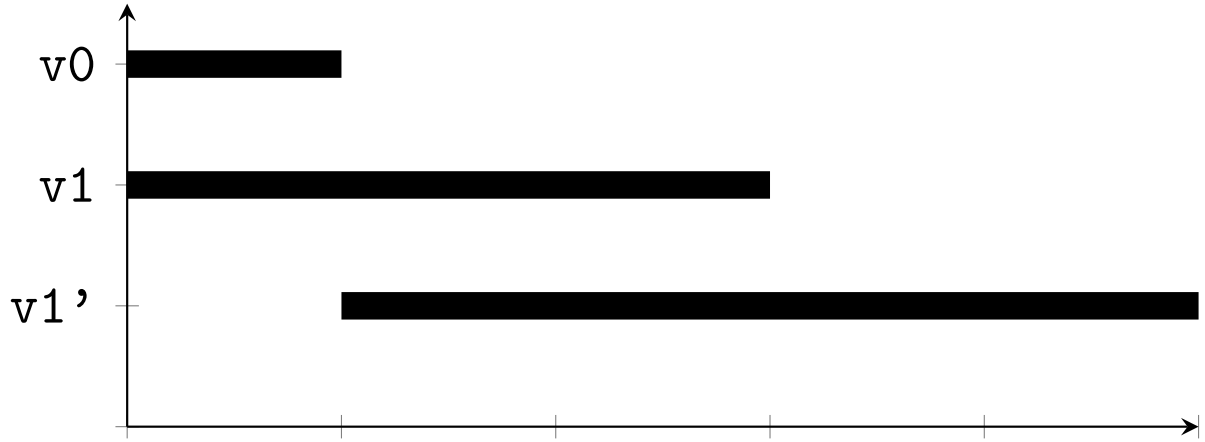

- Build interference graph G
  - Nodes represent live ranges
  - Edges represent interference between live ranges

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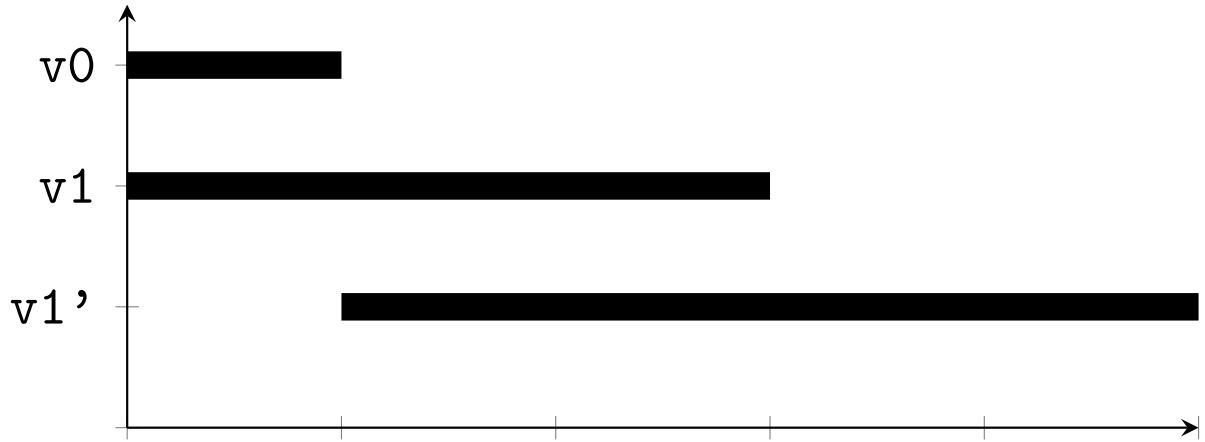

- Build interference graph G
  - Nodes represent live ranges
  - Edges represent interference between live ranges
- n-coloring exists if highest degree $< n$

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while *G has no n-coloring* **do**
  while $\exists v \in G$ *with* $\deg(v) < n$ **do**
    Remove v and its edges from G and push v on stack;
  end
  if $G = \emptyset$ **then**
    while *Stack* $\neq []$ **do**
      Pop v from stack, add v back to G;
      Color v;
    end
  else
    Choose a node v to spill;
    Remove v and its edges from G;
  end
end

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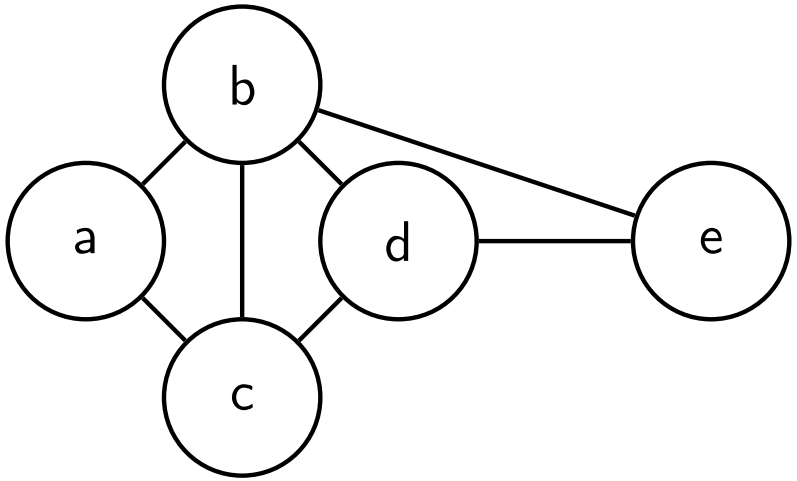

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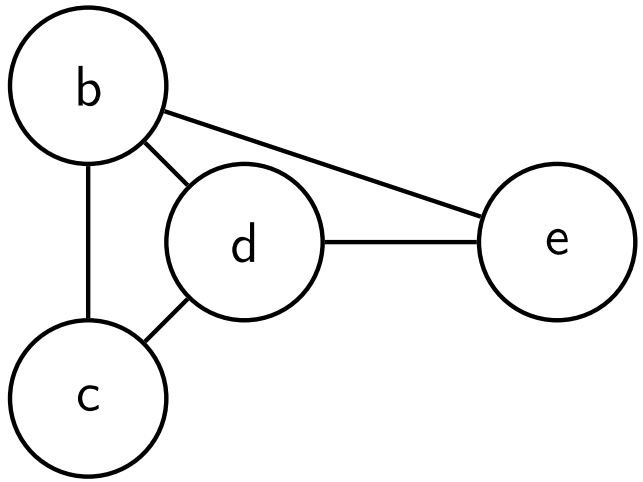

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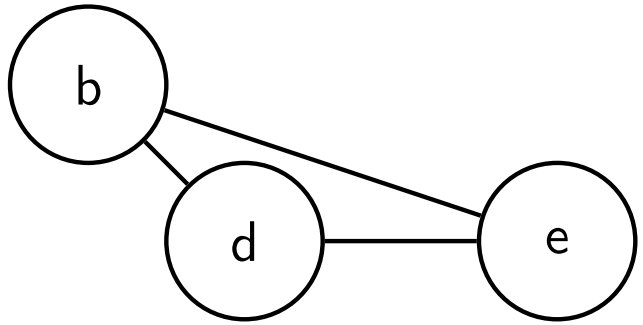

Stack $= [a, c]$

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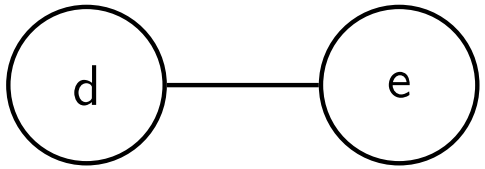

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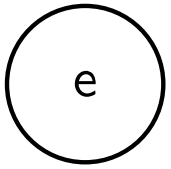

Stack $= [a, c, b, d]$

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Stack $= [a, c, b, d, e]$

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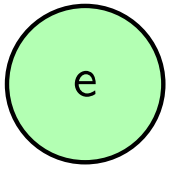

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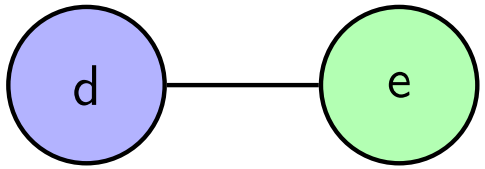

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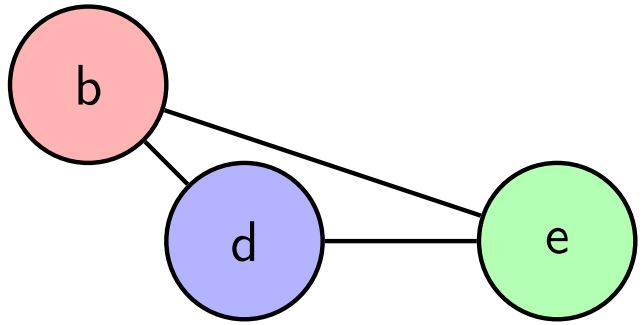

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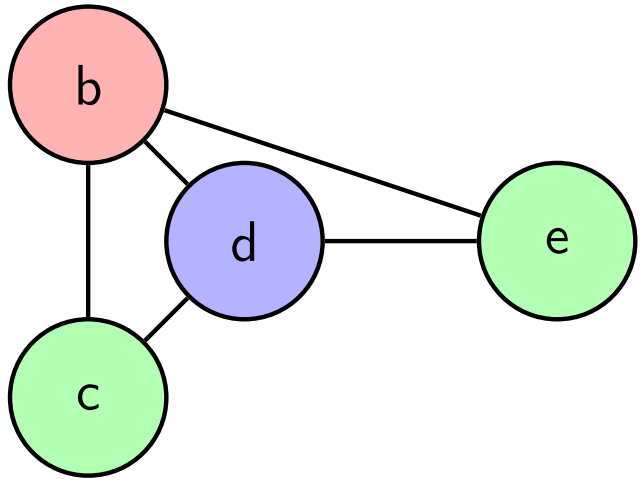

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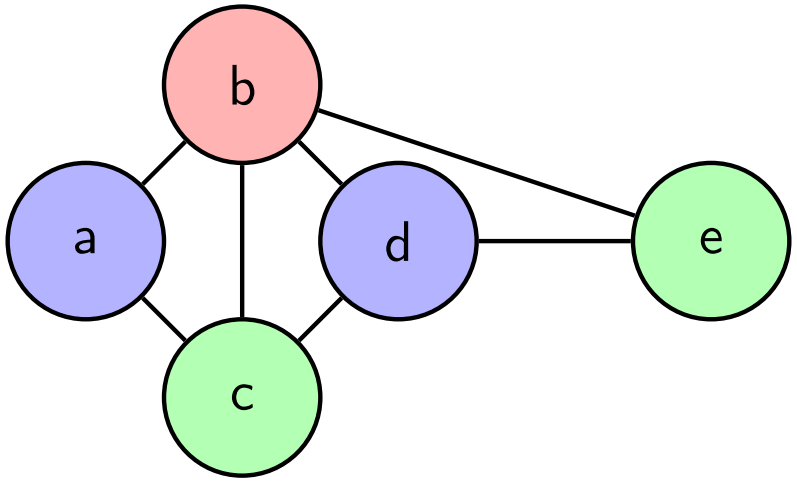

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- Many improvements
  - Rematerialization
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- Many improvements
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  - Live range splitting
- But still:
  - Multiple passes through program
  - Graph often rebuilt

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L = list of live ranges, sorted by start point;
A = list of allocated active live ranges;
foreach $l \in L$ **do**
    Remove expired live ranges from A, if any;
    if $length(A) = n$ **then**
        Choose live range $l' \in A$ that ends furthest away;
        Spill l', remove l' from A;
    end
    Allocate l, add l to A;
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- Generated code only $\approx 10\%$ slower

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- Region choice based on register pressure

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- Priority queue with spill weights
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- Accomodates architecture-specific preferences
  Thumb-2: 16-bit encoding when using `r0`–`r7`

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- Use 5.06 (June 2016) for comparison

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- n loads can be pipelined to take $n + 1$ cycles

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y14 =  U3 +  U5
y13 =  U0 +  U6
 y9 =  U0 +  U3
 y8 =  U0 +  U5
 t0 =  U1 +  U2
 y1 =  t0 +  U7
 y4 =  y1 +  U3
y12 = y13 + y14
 y2 =  y1 +  U0
 y5 =  y1 +  U6
 y3 =  y5 +  y8
 t1 =  U4 + y12
y15 =  t1 +  U5
y20 =  t1 +  U1
 y6 = y15 +  U7
y10 = y15 +  t0
```

```
y11 = y20 +  y9
 y7 =  U7 + y11
y17 = y10 + y11
y19 = y10 +  y8
y16 =  t0 + y11
y21 = y13 + y16
y18 =  U0 + y16
 t2 = y12 x y15
 t3 =  y3 x  y6
 t4 =  t3 +  t2
 t5 =  y4 x  U7
 t6 =  t5 +  t2
 t7 = y13 x y16
 t8 =  y5 x  y1
 t9 =  t8 +  t7
t10 =  y2 x  y7
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t14 = t13 + t12
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t17 =  t4 + y20
t18 =  t6 + t16
t19 =  t9 + t14
t20 = t11 + t16
t21 = t17 + t14
t22 = t18 + y19
t23 = t19 + y21
t24 = t20 + y18
t25 = t21 + t22
(...)
```


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- (Also, qhasm, but requires manual spill code generation)

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- Detect direct recomputation, can be cheaper than loading from memory
- Source code in public domain:
  `https://github.com/Ko-/aes-armcortexm`

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- (Excluding 32 loads for randomness)

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Algorithm	Speed (cycles)		ROM (bytes)		RAM (bytes)	
	M3	M4	Code	Data	I/O	Stack
AES-128-CTR	546.3	**554.4**	2192	1024	192 $+2m$	72
Bitsliced AES-128-CTR	1616.6	**1617.6**	12120	12	368 $+2m$	108
Masked bitsliced AES-128-CTR	N/A	**7422.6**	39916	12	368 $+2m$	1588
AES-128 KS	289.8	294.8	902	1024	176	32
Bitsliced AES-128 KS	1027.8	1033.8	3434	1036	368	188
Masked bitsliced AES-128 KS	1027.8	1033.8	3434	1036	368	188

More on full AES in [SS16]

Thanks. . .

. . . for your attention!

Paper and code at
https://ko.stoffelen.nl/

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